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1. A memory device, comprising:

a substrate;

a plurality of self-aligned nano-rectifying elements, having:

a plurality of first electrode lines disposed over said substrate,

a plurality of device structures disposed on said plurality of first electrode lines forming said plurality of self-aligned nano-rectifying elements, each device structure having at least one lateral dimension less than about 75 nanometers;

a plurality of switching elements, said switching elements disposed over and self-aligned in at least one direction with said device structures; and

a plurality of second electrode lines disposed over, electrically coupled to, and self-aligned to said switching elements, whereby a memory device is formed.

2. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of first semiconductor lines including a dopant of a first polarity.

3. The memory device in accordance with claim 2, wherein said plurality of first semiconductor lines further comprises a plurality of first epitaxial semiconductor lines.

4. The memory device in accordance with claim 2, wherein said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant of a second polarity, wherein each semiconductor device structure forms a semiconductor junction with one of said plurality of first semiconductor lines, said semiconductor junction having an area with at least one lateral dimension less than about 75 nanometers.

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5. The memory device in accordance with claim 2, wherein said plurality of semiconductor device structures further comprises a plurality of epitaxial semiconductor device structures.

6. The memory device in accordance with claim 2, wherein each device structure of said plurality of device structures further comprises:

an intrinsic semiconductor structure disposed on one of said plurality of first semiconductor lines; and

a second semiconductor device structure including a dopant of a second polarity, disposed on said intrinsic semiconductor structure, wherein said intrinsic semiconductor structure and said second semiconductor device structure each have at least one lateral dimension less than about 75 nanometers, whereby a plurality of p-i-n diode elements are formed.

7. The memory device in accordance with claim 2, wherein said plurality of first semiconductor lines is formed on an insulating layer formed on said substrate.

8. The memory device in accordance with claim 7, wherein said insulating layer is selected from the group consisting of SiOx, SixNy, SiOxNy, SixCy, and mixtures thereof.

9. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of metal electrode lines, and wherein said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant, forming a plurality of Schottky barrier contacts between said plurality of metal electrode lines and said plurality of semiconductor device structures, each Schottky barrier contact having an area with at least one lateral dimension less than about 75 nanometers.

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10. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of metal electrode lines, and wherein each device structure further comprises:

a dielectric layer disposed on one of said plurality of metal electrode lines; and

a metal layer disposed on said dielectric layer, forming a plurality of metal-insulator-metal rectifying elements, wherein each metal-insulator-metal rectifying element having at least one lateral dimension less than about 75 nanometers.

11. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a ferroelectric material.

12. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a phase change material.

13. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a filament forming material.

14. The memory device in accordance with claim 13, wherein said filament forming material is selected from the group consisting of As_2Se_3:Ag, Cu_2S, InSe, and mixtures thereof.

15. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises an organic or polymer layer.

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16. The memory device in accordance with claim 15, wherein said organic layer further comprises a self-assembled monolayer of organic molecules.

17. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a piezoelectric material.

18. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a chalcogenide material.

19. The memory device in accordance with claim 1, wherein said plurality of first electrode lines are substantially parallel to each other.

20. The memory device in accordance with claim 19, wherein said plurality of switching elements further comprises a plurality of switching lines substantially parallel to each other.

21. The memory device in accordance with claim 20, wherein said plurality of switching lines are substantially mutually orthogonal to said plurality of first electrode lines.

22. The memory device in accordance with claim 1, wherein each device structure has an area less than about 5,625 square nanometers.

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23. A memory device, comprising:

a substrate;

a first plurality of conductive lines substantially parallel to each other disposed on said substrate;

a plurality of semiconducting junctions formed on said first plurality of conductive lines, said junctions having at least one lateral dimension less than about 75 nanometers;

a second plurality of conductive lines substantially parallel to each other and substantially mutually orthogonal to said plurality of semiconducting lines; and

a storage media disposed between said first and said second conductive lines and electrically coupled to said junctions and said second plurality of conductive lines.

24. A memory device comprising:

a substrate;

means for rectifying including a first plurality of conductive lines substantially parallel to each other disposed on said substrate, said means for rectifying self-aligned with said plurality of conductive lines, wherein said means for rectifying having at least one lateral dimension less than about 75 nanometers;

means for storing a data bit in each of a plurality of storage elements disposed over said first plurality of conductive lines and self-aligned to said means for rectifying; and

means for electrically addressing said plurality of storage elements, wherein each storage element self-aligned with said means for electrically addressing, and wherein each intersection of said means for electrically addressing and said first plurality of conductive lines defines a logic cell, of a memory structure.

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25. A memory device, comprising:

a substrate;

a plurality of rectifying structures, disposed on said substrate, said rectifying structures form an i x j array, wherein i and j are integer values, each rectifying structure having at least one lateral dimension less than about 75 nanometers;

a plurality of storage media elements, each storage media element disposed on and electrically coupled to one of said rectifying structures, each storage media element having at least one lateral dimension less than about 75 nanometers; and

a plurality of electrical conductor lines disposed on and electrically coupled to said plurality of storage media elements, wherein each storage media element is self-aligned to one of said rectifying structures and is self-aligned to one of said electrical conductor lines.

26. A memory device, comprising:

a substrate;

a plurality of self-aligned nano-rectifying elements, having:

a plurality of first conductive lines disposed over said substrate, each first conductive line having at least one lateral dimension less than about 75 nanometers,

a plurality of device structures disposed on said plurality of first conductive lines, each device structure having at least one lateral dimension less than about 75 nanometers, wherein the combination of said first conductive lines and said device structures forms said plurality of nano-rectifying elements;

a plurality of switching elements, each switching element disposed on and electrically coupled to one of said plurality of device structures; and

a plurality of second conductive lines, said second conductive lines electrically coupled to said plurality of switching elements, each second conductive line intersects with at least one first conductive line, wherein each

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nano-rectifying element is substantially facially coextensive, coincident, and coplanar with one of said plurality of first conductive lines and one of said plurality of switching elements.

27. A memory device, comprising:

a substrate;

a plurality of semiconducting lines including a dopant of a first polarity said semiconducting lines substantially parallel to each other and disposed over said substrate;

a plurality of semiconducting structures including a dopant of a second polarity disposed on said plurality of semiconducting lines;

a plurality of junctions formed between said lines and said semiconducting structures said junctions having at least one lateral dimension less than about 75 nanometers;

a switching element disposed on and electrically coupled to said semiconducting structures; and

a plurality of electrical conductors substantially parallel to each other, coupled to said storage media and substantially mutually orthogonal to said plurality of semiconducting lines.

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